LAYOUT OF DRIVER SETS IN A CROSS POINT MEMORY ARRAY

S/N 10/612,733
Filed 07/01/2003
Docket # P015.03.ABC

Inventors:

Darrell Rinerson
Christophe J. Chevallier
Steven W. Longcor
Wayne Kinney
Edmond R. Ward
Steve Kuo-Ren Hsia

and incorporated by reference in paragraph 0017 of SN 10/773,549

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/400,849, filed August 02, 2002, the U.S. Provisional Application No. 60/422,922, filed October 31, 2002, and the U.S. Provisional Application 60/424,083, filed November 5, 2002, all of which are incorporated herein by reference in their entireties and for all purposes. This application is related to the following U.S. Patent Applications: U.S. Application No. 10/360,005, filed February 7, 2003; U.S. Application No. 10/330,512, filed December 26, 2002; Application No. 10/330,153, filed December 26, 2002; Application No. 10/330,964, filed December 26, 2002; Application No. 10/330,170, filed December 26, 2002; Application No. 10/330,900, filed December 26, 2002; Application No. 10/330,150, filed December 26, 2002; Application No. 10/330,965, filed December 26, 2002; and the applications that are titled "RAM With Multiple Memory Layers Using Shared Logic," "Line Drivers That Fit Within A Specified Line Pitch," "Cross Point Memory Array With Fast Access Time," and "Line Drivers That Use Minimal Metal Layers," all of which are filed on date herewith. All of the above applications are hereby incorporated herein by reference in their entireties and for all purposes.

PAGE 3/12 * RCVD AT 2/1/2006 1:39:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:14087378067 * DURATION (mm-ss):02-32

SUMMARY OF THE INVENTION

[0012] The present invention provides for various layouts of driver sets in a re-writable memory that uses a cross point array. The re-writable memory includes a semiconductor substrate, a cross point array and both x-direction and y-direction driver sets. The cross point memory array is formed above the semiconductor substrate and includes at least one layer of memory plugs, at least one x-direction conductive layer and at least one y-direction conductive layer. The driver sets are formed on the semiconductor substrate and driver the conductive layers. An x-direction driver set drives the x-direction conductive layer and a y-direction driver set drives the y-direction conductive layer.

[0013] In another aspect of the invention, various driver sets are underneath the cross point array. While interdigitated driver sets will typically have at least a portion of the driver sets that fall outside of the cross point array, some non-interdigitated layouts can have all of the driver sets placed underneath the memory.

PAGE 4/12 * RCVD AT 2/1/2006 1:39:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:14087378067 * DURATION (mm-ss):02-32

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may best be understood by reference to the following description taken in conjunction with the accompanying drawings, in which:

Figure 1 depicts a perspective view of an exemplary cross point memory array employing a single layer of memory;

Figure 2 depicts a side view of an exemplary memory plug with five layers and sandwiched between two conductive array lines;

Figure 3A illustrates selection of a memory cell in the cross point array depicted in figure 1;

Figure 3B illustrates the boundaries of the selected memory cell of figure 3A;

Figure 4A depicts a perspective view of an exemplary stacked cross point memory array employing four layer of memory;

Figure 4B depicts a schematic diagram of the stacked cross point memory of figure 4A;

Figure 5 depicts a cross section of the stacked cross point array of figure 4A;

Figure 6A depicts a schematic diagram of x-direction driver sets in conjunction with the stacked cross point memory of figure 4A;

Figure 6B depicts a schematic diagram of y-direction driver sets in conjunction with the stacked cross point memory of figure 4A;

Figure 7A depicts the general layout of the x-direction and y-direction driver sets depicted in figures 6A and 6B in relation to the stacked cross point array depicted in figure 4A;

Figure 7B depicts an abstracted representation of figure 7A;

PAGE 5/12 * RCVD AT 2/1/2006 1:39:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:14087378067 * DURATION (mm-ss):02-32

* Figure 8A depicts the general layout of interdigitated x-direction and y-direction driver in relation to the single layer cross point array depicted in figure 1;

* Figure 8B depicts an abstracted representation of figure 8A;

Figure 9A depicts the general layout of interdigitated x-direction and y-direction driver in relation to the stacked cross point array depicted in figure 4A;

Figure 9B depicts an abstracted representation of figure 8A;

Figures 10A and 10B depicts a schematic diagram of alternating x-direction driver sets in conjunction with the stacked cross point memory of figure 4A;

Figures 11A through 11C depict various layouts of the x-direction and y-direction driver sets that have some drivers underneath the single-layer cross point array depicted in figure 1;

Figure 12 depicts a layout of the x-direction and y-direction driver sets that interdigitate some drivers but not others such that some drivers are underneath the single-layer cross point array depicted in figure 1;

Figure 13A depicts a layout of an x-direction driver set and a y-direction driver set that completely fits underneath the single-layer cross point array depicted in figure 1;

Figure 13B depicts another layout of an x-direction driver set and a y-direction driver set that completely fits underneath the single-layer cross point array depicted in figure 1;

Figure 14A depicts a layout of x-direction driver sets and a y-direction driver sets that completely fits underneath the stacked cross point array depicted in figure 4A;

Figure 14B depicts a layout of x-direction driver sets and a y-direction driver sets that leaves empty gaps underneath the single-layer cross point array depicted in figure 4A;

PAGE 6/12 * RCVD AT 2/1/2006 1:39:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:14087378067 * DURATION (mm-ss):02-32

[0044] The thru 505 that connects the X_1 layer 430 to the peripheral circuitry would go through at least two inter-layer dielectric (ILD) layers 515 and 520. ILD layers provide several functions, including preventing capacitive coupling between conductive array lines and providing a substrate for conductive array lines that would otherwise need to span empty spaces.

[0045] The thru 510 that connects the X_2 layer 435 to the peripheral circuitry would go through at least four ILD layers 515, 520, 525, and 530. Although thrus 505 and 510 may be formed during the same processing steps as the memory layers, a conductive material 535 would need to be used to connect the conductive array lines to the peripheral circuitry.

The Peripheral Circuitry

[0046] Figure 6A depicts x-direction driver sets 605, 610, and 615 that are used to select specific x-direction conductive array lines in the X_0 layer 425, X_1 layer 430, and X_2 layer 435. Although the X_0 driver 605 and the X_2 driver 615 can use identical logic (as described in table 1), separate drivers are shown because of the difficulty in routing the single X_0 driver 605 around the thru 505 that connects the X_1 layer 430 to the X_1 driver 610.

[0047] Figure 6B depicts y-direction driver sets 620 and 625 that are used to select specific y-direction conductive array lines in the y-direction conductive array line layers 440 and 445. The Y_0 driver set 620 uses a thru 630 that goes through one ILD layer 515 in order to connect with the Y_0 layer 440. The Y_1 driver set 625 uses a thru 635 that goes through three ILD layers 515, 520, and 525 in order to connect with the Y_1 layer 445.

PAGE 7/12 * RCVD AT 2/1/2006 1:39:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:14087378067 * DURATION (mm-ss):02-32

[0048] Figure 7A depicts the general layout of the x-direction and y-direction driver sets 605, 610, 615, 620, and 625 in relation to the stacked cross point array 400. Figure 7B is a more abstracted representation of figure 7A. Since each driver set is on the same side the entire layout forms a non-symmetrical L-shape.

[0049] However, certain designs may interdigitate the driver circuitry so that the driver that controls one conductive array line comes from one side and the driver that controls the next conductive array line comes from the opposite side.

Interdigitated Driver Sets

[0050] Figures 8A and 8B depict a layout of an interdigitated x-direction driver 805 and an interdigitated y-direction driver 810 that drive a single-layer cross point array 100. Interdigitating the drivers 805 and 810 not only allows for greater symmetry in a single-layer cross point array 100, but also permits the drivers to be fabricated to thicker dimensions. Interdigitation can additionally be used for stacked cross point arrays.

[0051] Drivers can be considered to be interdigitated when alternating lines in the same conductive array line layer are driven from different locations. For example, even numbered lines can be driven from one side and odd numbered lines can driven from the opposite side. Conductive array lines can also be interdigitated in groups, for example having Such oppositely driven lines may be alternate, i.e. alternately a line driven from one side and a line driven from the other side, or grouped by pair, where 2 lines driven from one side are adjacent and two lines driven from the other side are next to them, or grouped in any arrangement which allows the use of a driver which is laid out in the pitch of 2 x N cells, and drives N lines. By extension, we call

PAGE 8/12 * RCVD AT 2/1/2006 1:39:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:14087378067 * DURATION (mm-ss):02-32

"interdigitated driver set" a set of drivers driving interdigitated lines even though the drivers themselves are not interdigitated.

[0052] Figures 9A and 9B depict a layout of driver sets 605, 610, 620, and 625 for the stacked cross point array 400 that are interdigitated. The configuration of the x-direction driver sets 605 and 610 are depicted in figures 10A and 10B. The configuration of figure 10A is alternated with the configuration of figure 10B for each x-direction conductive array line so that both the X_0 driver 605 and the X_1 driver 610 alternate sides.

[0053] Additionally, by placing the thru 505 that connects the X_1 layer 430 to the X_1 driver 610 and thru 510 that connects the X_2 layer 435 to the X_0 driver 605 on opposite sides, the bottom X_0 layer 425 can be directly tied to the X_2 layer 435. Therefore, a single X_0 driver 605 can be used for both the bottom X_0 layer 425 and the top X_2 layer 435.

[0054] The layouts shown in figures 7B, 8B and 9B assume that the drivers 605, 610, 615, 620, 625, 805, and 810 all lie outside the cross point array 100 or 400. However, if the substrate underneath the cross-point array 100 or 400 is used to draw the peripheral circuitry, the footprint of the entire memory chip can be reduced.

[0055] Figures 11A through 11C depict various layouts of the x and y direction driver sets 805 and 810 that have some drivers underneath the single-layer cross point array 100. In each layout, some drivers are left outside of the single-layer cross point array 100 even though there may be unused space underneath the cross point array 100. In figure 11A the layout forms a rectangle that extends beyond the cross point array 100 in the x-direction. In figure 11B the layout forms an H-shape that extends beyond the cross point array 100 in the y-direction. In figure 11C the layout forms a

PAGE 9/12 * RCVD AT 2/1/2006 1:39:27 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:14087378067 * DURATION (mm-ss):02-32